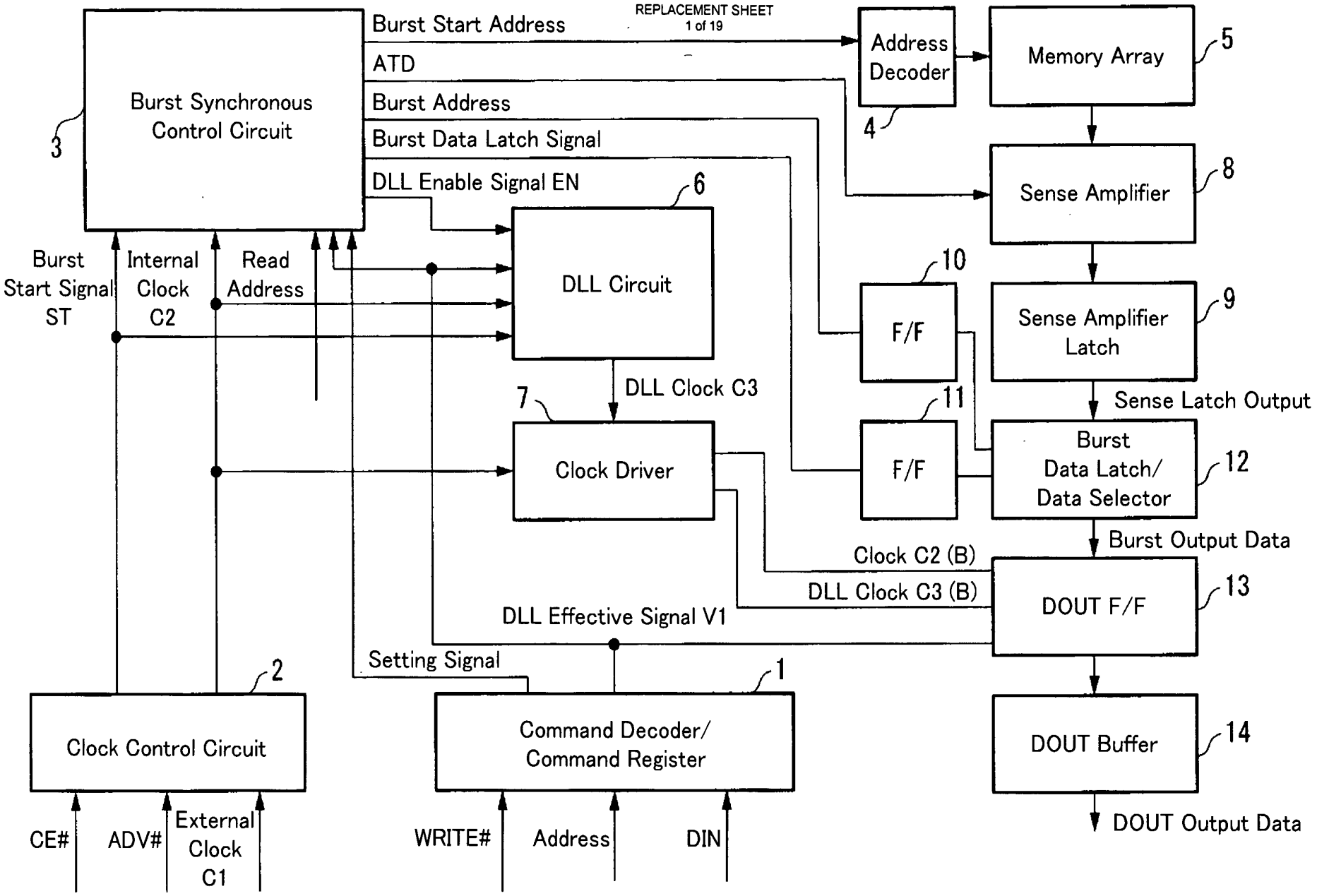
Burst Synchronous Control Circuit
3
Burst Start Address
ATD
Burst Address
Burst Data Latch Signal
DLL Enable Signal EN
Address Decoder
4
Memory Array
5
Sense Amplifier
8
6
DLL Circuit
10
F/F
Sense Amplifier Latch
9
Burst Start Signal ST
Internal Clock C2
Read Address
DLL Clock C3
7
Clock Driver
11
F/F
Sense Latch Output
Burst Data Latch/ Data Selector
12
Burst Output Data
Clock C2 (B)
DLL Clock C3 (B)
DOUT F/F
13
DLL Effective Signal V1
Setting Signal
2
Clock Control Circuit
1
Command Decoder/ Command Register
DOUT Buffer
14
CE#
ADV#
External Clock C1
WRITE#
Address
DIN
DOUT Output Data

Fig. 1

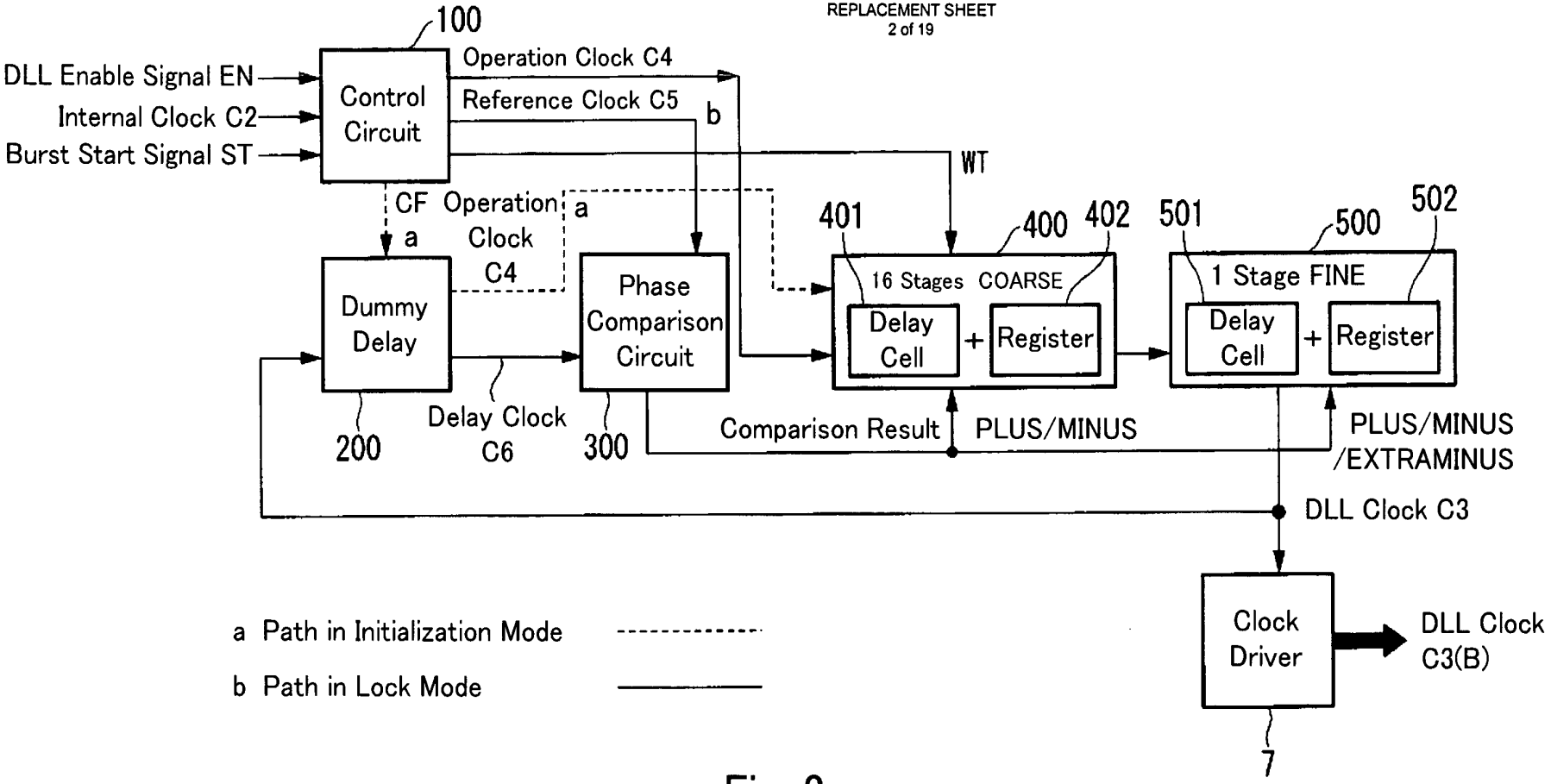
100
DLL Enable Signal EN
Internal Clock C2
Burst Start Signal ST
Control Circuit
Operation Clock C4
Reference Clock C5
b
WT
CF
a
Operation Clock C4
a
Dummy Delay
Phase Comparison Circuit
401
400
402
16 Stages COARSE
Delay Cell
+
Register
501
500
502
1 Stage FINE
Delay Cell
+
Register
200
Delay Clock C6
300
Comparison Result
PLUS/MINUS
PLUS/MINUS /EXTRAMINUS
DLL Clock C3
Clock Driver
DLL Clock C3(B)
7
a Path in Initialization Mode
b Path in Lock Mode

Fig. 2

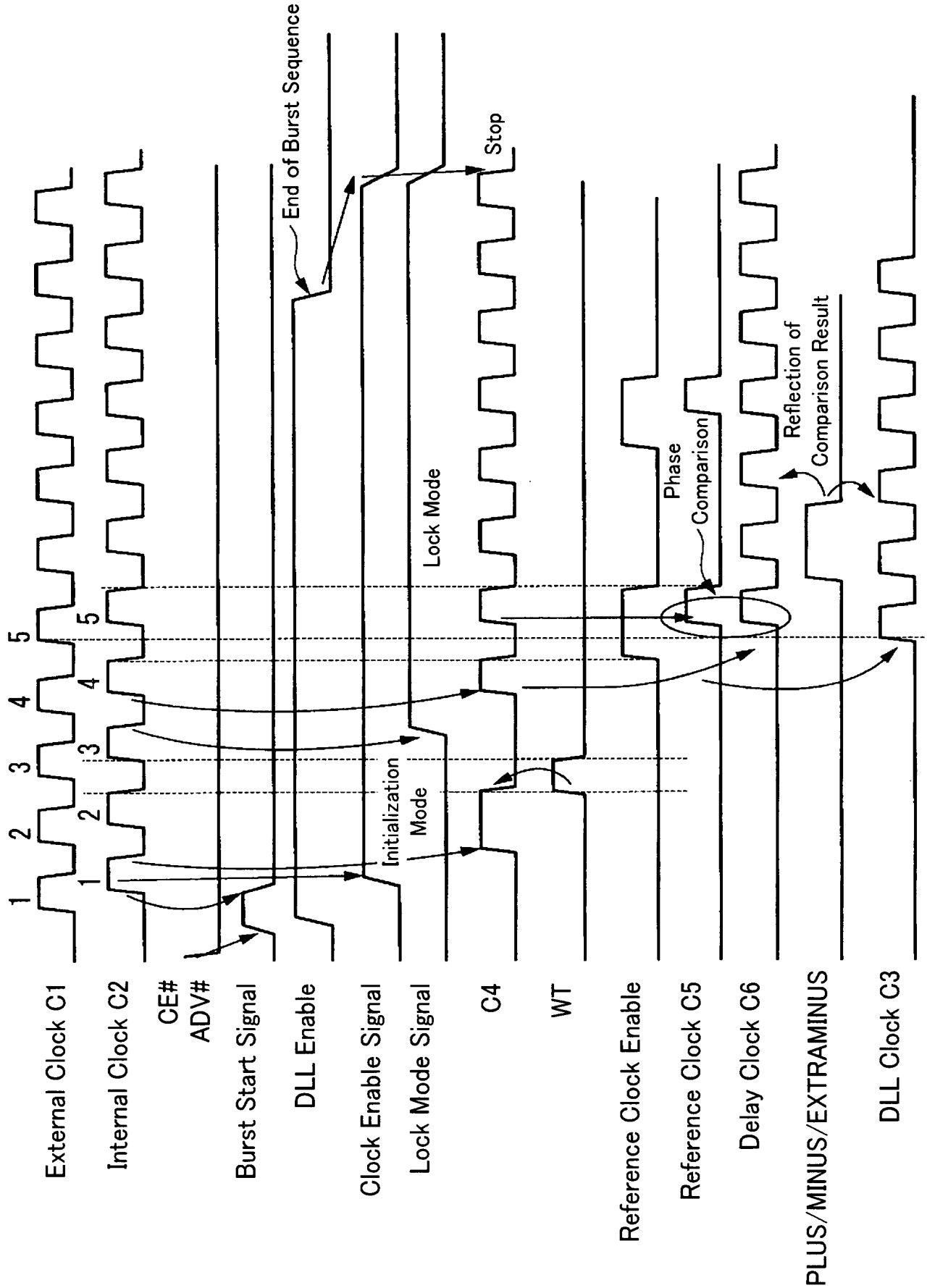
External Clock C1
Internal Clock C2
CE#
ADV#
Burst Start Signal
DLL Enable
Clock Enable Signal
Lock Mode Signal
C4
WT
Reference Clock Enable
Reference Clock C5
Delay Clock C6
PLUS/MINUS/EXTRAMINUS
DLL Clock C3
1
2
3
4
5
1
2
3
4
5
End of Burst Sequence
Stop
Initialization Mode
Lock Mode
Phase Comparison
Reflection of Comparison Result

Fig. 3

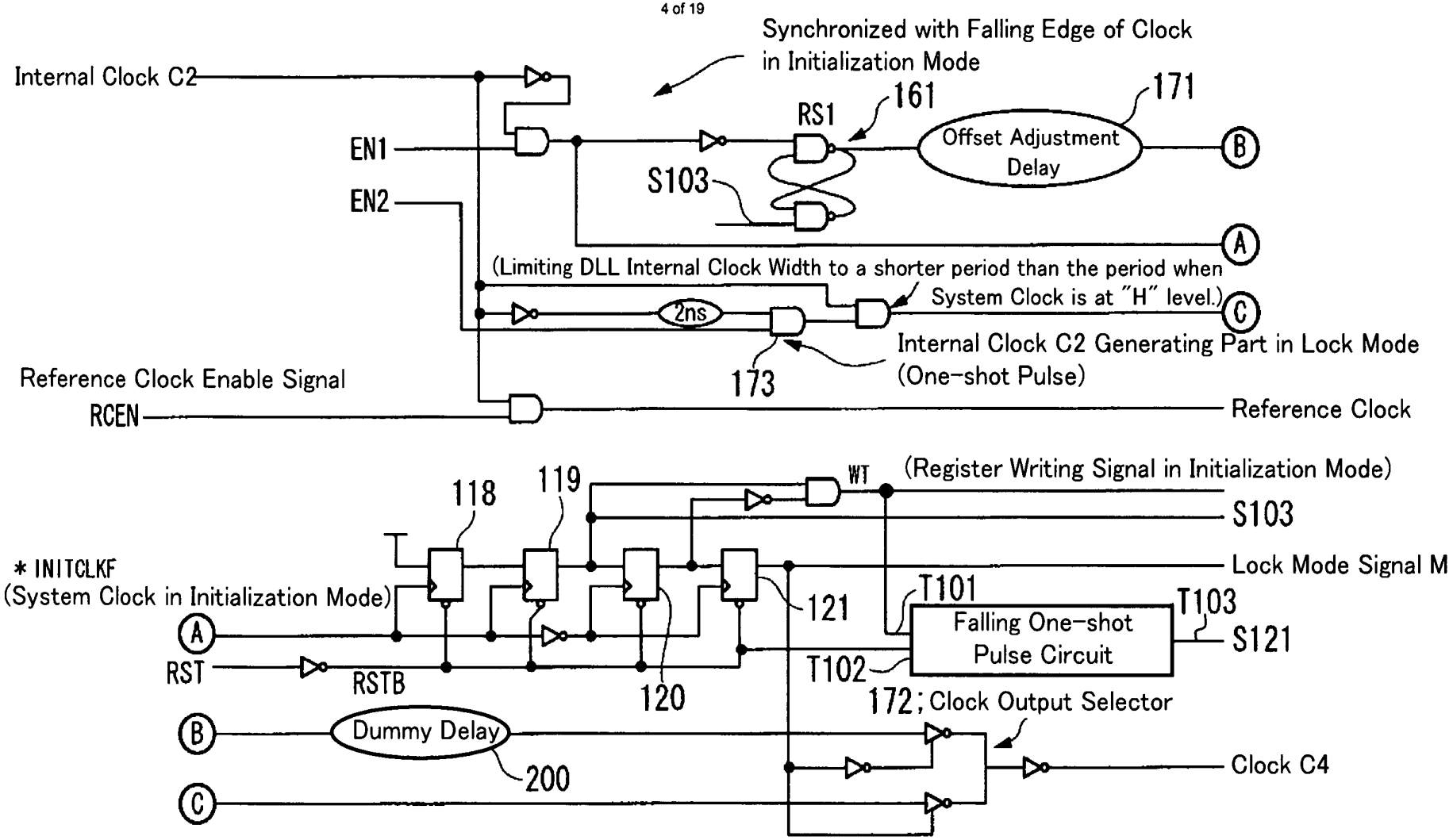
Synchronized with Falling Edge of Clock in Initialization Mode
Internal Clock C2
EN1
EN2
RS1
161
171
Offset Adjustment Delay
S103
B
A
(Limiting DLL Internal Clock Width to a shorter period than the period when System Clock is at "H" level.)
2ns
C
Internal Clock C2 Generating Part in Lock Mode (One-shot Pulse)
173
Reference Clock Enable Signal
RCEN
Reference Clock
WT
(Register Writing Signal in Initialization Mode)
118
119
S103
* INITCLKF
(System Clock in Initialization Mode)
Lock Mode Signal M
121
T101
T103
Falling One-shot Pulse Circuit
S121
A
RST
RSTB
120
T102
172; Clock Output Selector
B
Dummy Delay
200
Clock C4
C

Fig. 4

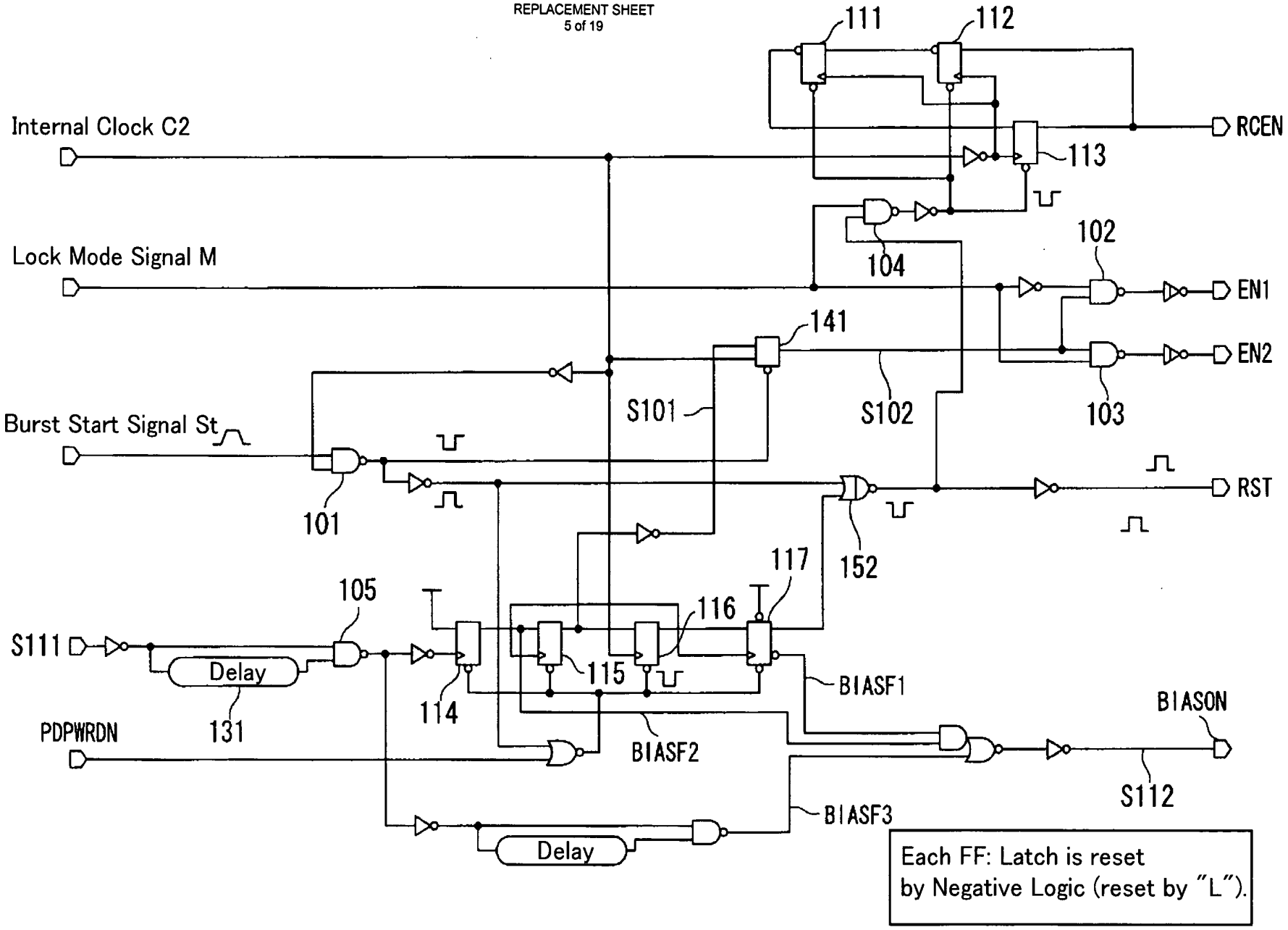
Internal Clock C2
Lock Mode Signal M
Burst Start Signal St
S111
PDPWRDN
Delay
131
101
105
114
115
116
117
141
S101
S102
152
102
104
103
EN1
EN2
RCEN
113
RST
BIASF1
BIASF2
BIASF3
BIASON
S112
Delay
Each FF: Latch is reset
by Negative Logic (reset by "L").

Fig. 5

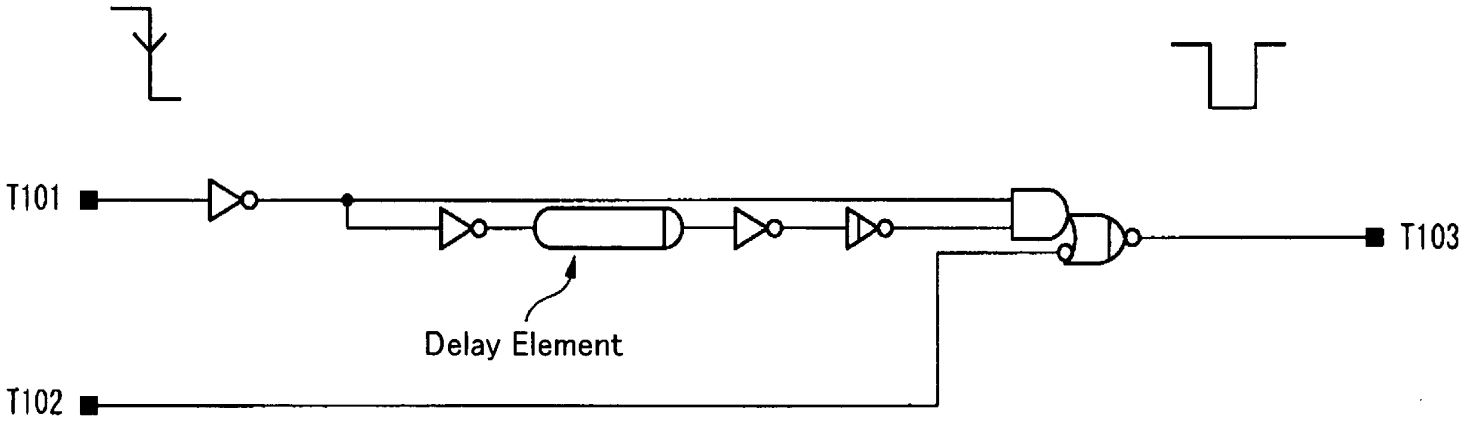

Fig. 6

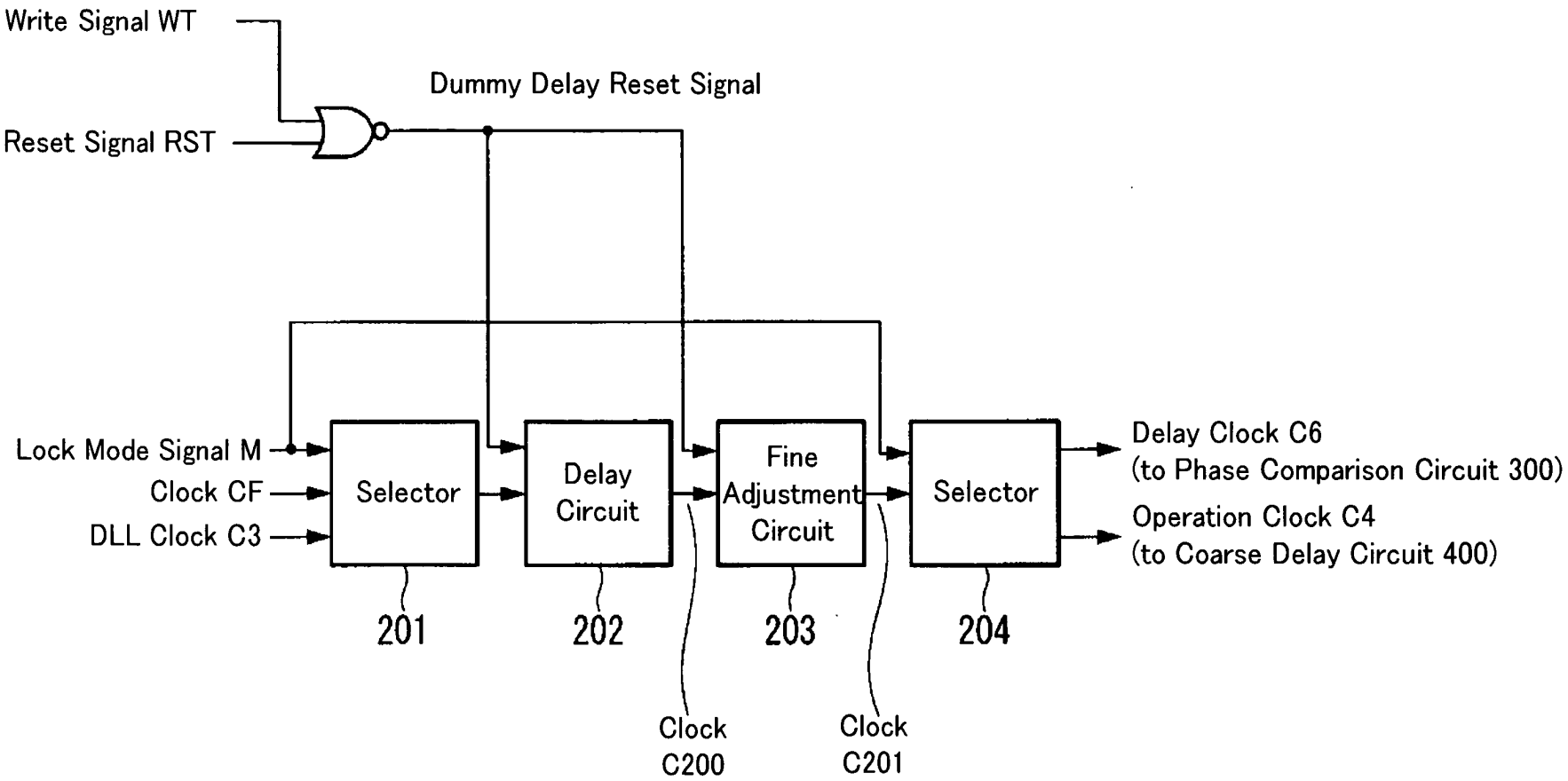
Write Signal WT
Dummy Delay Reset Signal
Reset Signal RST
Lock Mode Signal M
Clock CF
DLL Clock C3
Selector
Delay Circuit
Fine Adjustment Circuit
Selector
Delay Clock C6
(to Phase Comparison Circuit 300)
Operation Clock C4
(to Coarse Delay Circuit 400)
201
202
203
204
Clock C200
Clock C201

Fig. 7

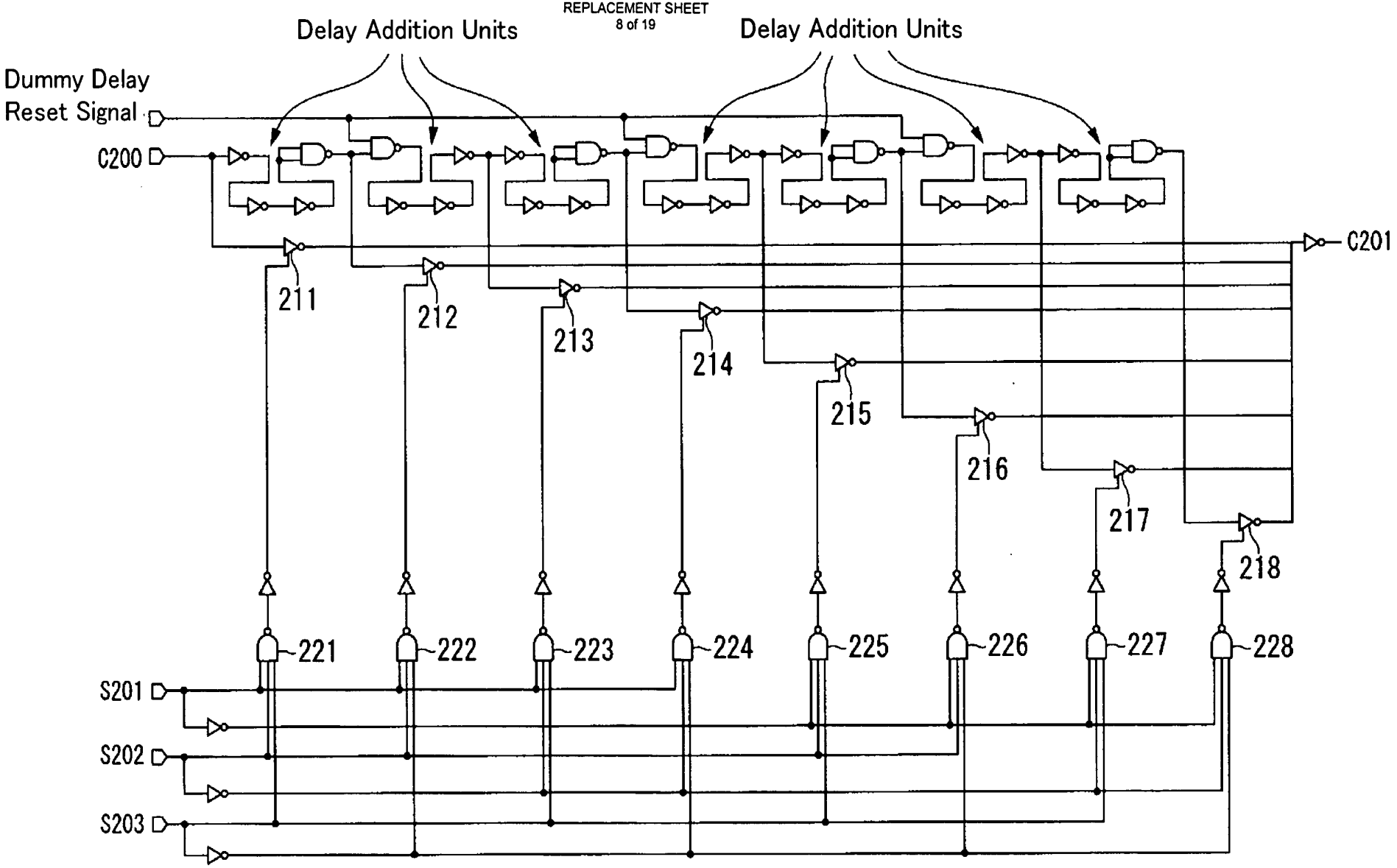
Delay Addition Units
Delay Addition Units
Dummy Delay
Reset Signal
C200
C201
211
212
213
214
215
216
217
218
221
222
223
224
225
226
227
228
S201
S202
S203

Fig. 8

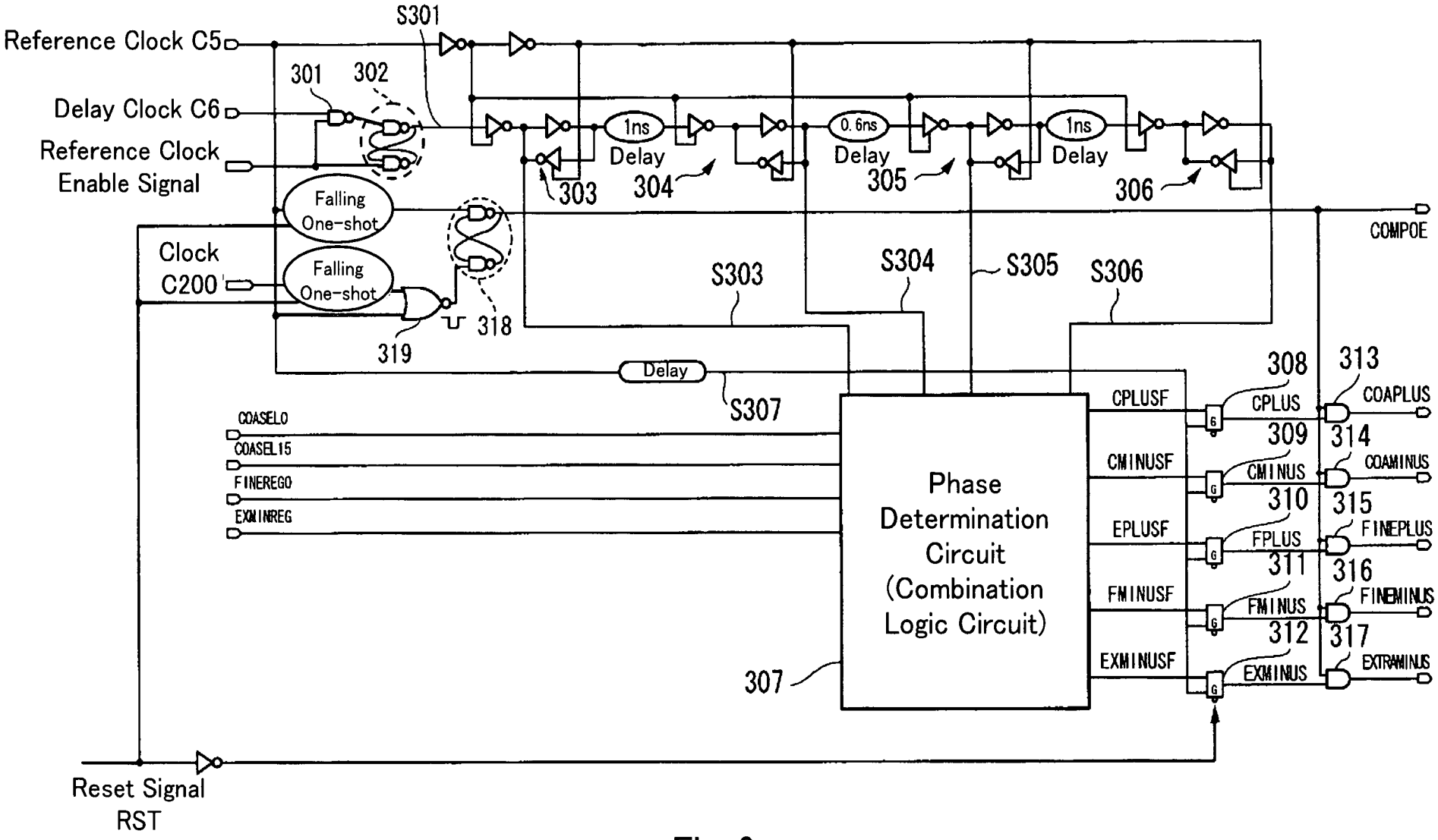
Reference Clock C5
Delay Clock C6
Reference Clock Enable Signal
Clock C200
Reset Signal RST
S301
301
302
303
304
305
306
1ns Delay
0.6ns Delay
1ns Delay
Falling One-shot
Falling One-shot
318
319
Delay
S307
S303
S304
S305
S306
COMPOE
COASEL0
COASEL15
FINEREG0
EXMINREG
Phase Determination Circuit (Combination Logic Circuit)
307
CPLUSF
CMINUSF
EPLUSF
FMINUSF
EXMINUSF
308
CPLUS
309
CMINUS
310
FPLUS
311
FMINUS
312
EXMINUS
313
COAPLUS
314
COAMINUS
315
FINEPLUS
316
FINEMINUS
317
EXTRAMINUS

Fig. 9

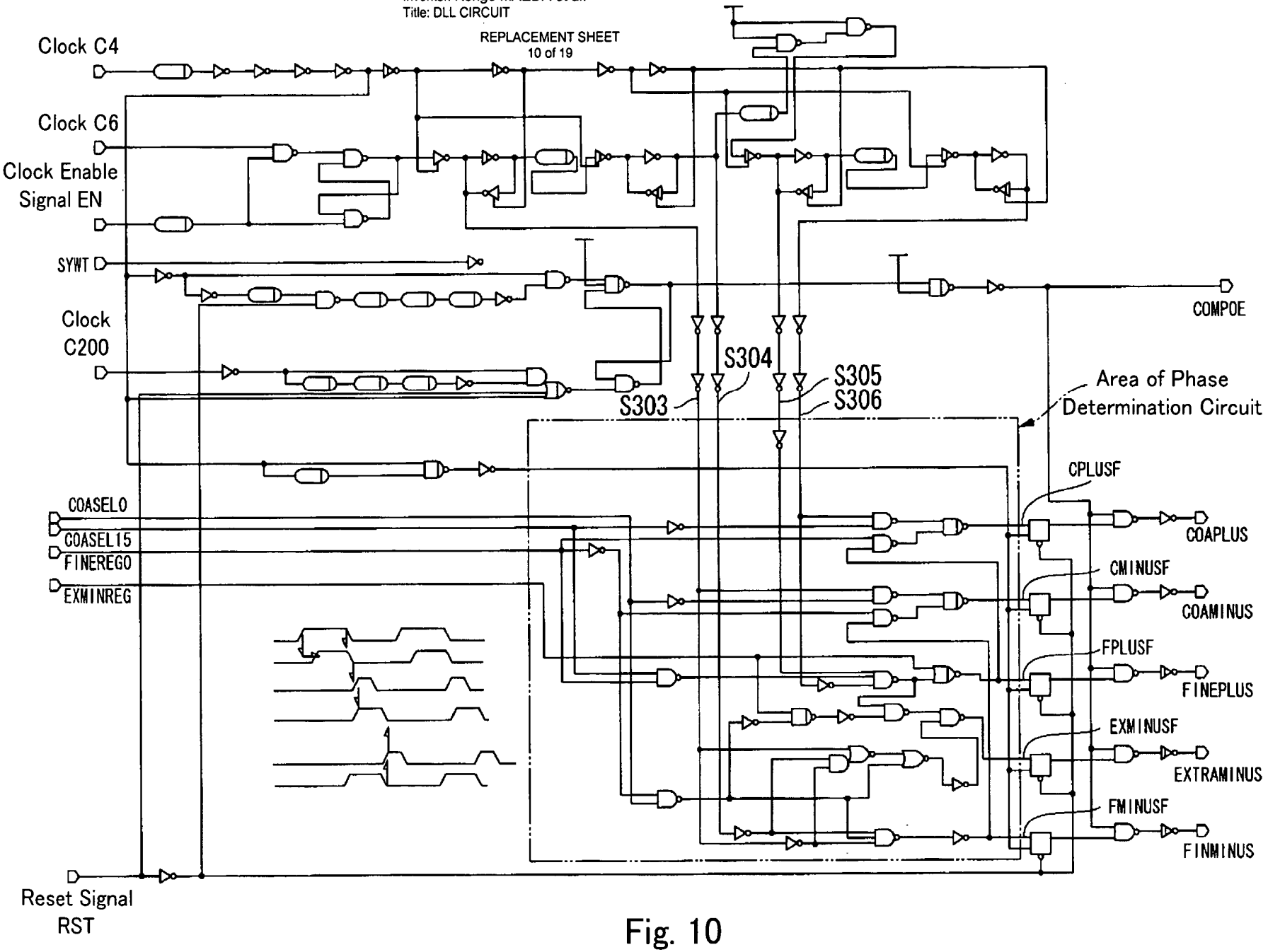
Clock C4
Clock C6
Clock Enable Signal EN
SYWT
Clock C200
COMPOE
S303
S304
S305
S306
Area of Phase Determination Circuit
CPLUSF
COASEL0
COASEL15
FINEREG0
EXMINREG
COAPLUS
CMINUSF
COAMINUS
FPLUSF
FINEPLUS
EXMINUSF
EXTRAMINUS
FMINUSF
FINMINUS
Reset Signal RST

Fig. 10

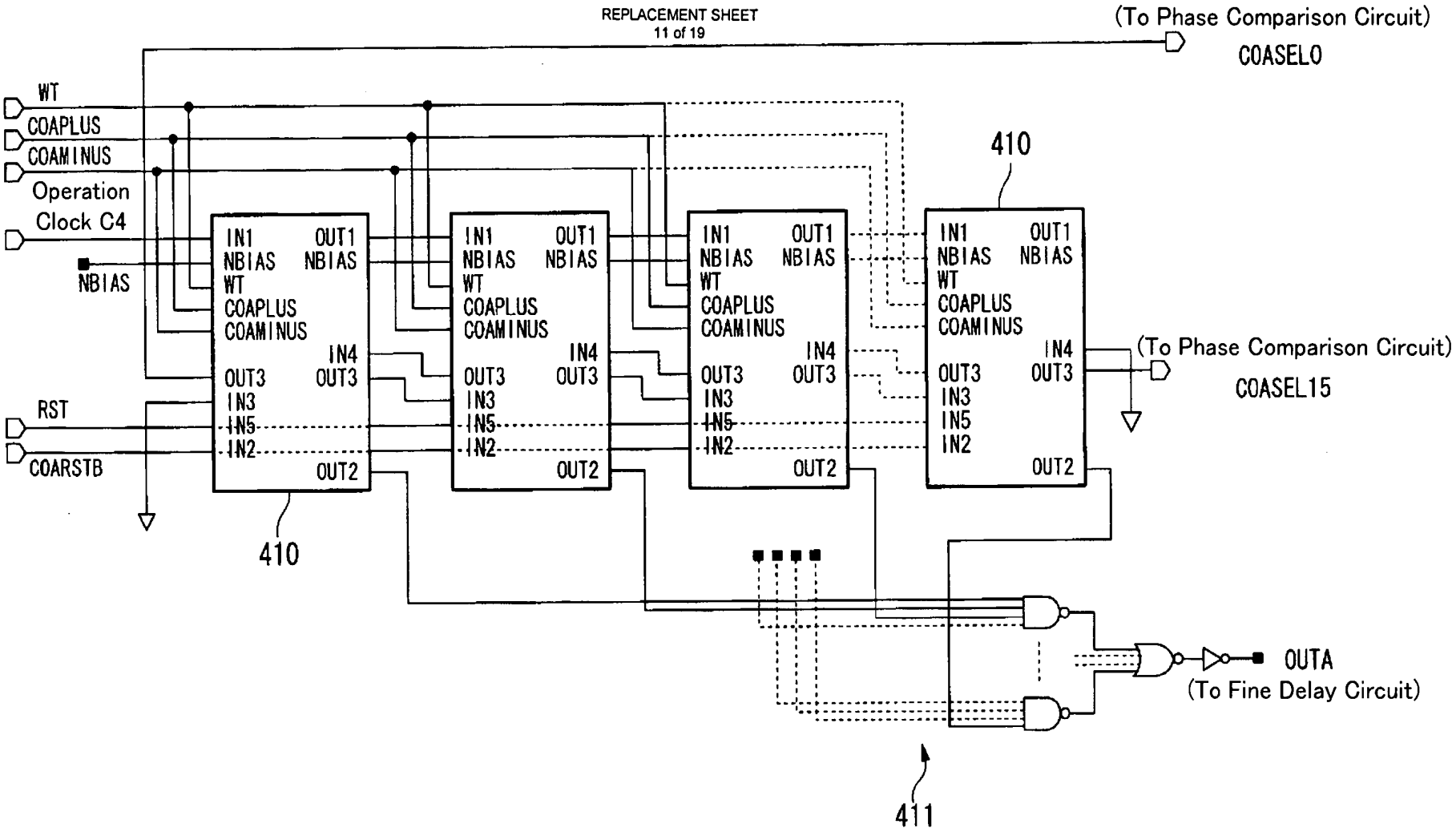
(To Phase Comparison Circuit)
COASEL0
WT
COAPLUS
COAMINUS
Operation
Clock C4
NBIAS
RST
COARSTB
IN1
NBIAS
WT
COAPLUS
COAMINUS
IN4
IN3
IN5
IN2
OUT1
NBIAS
OUT3
OUT2
410
410
(To Phase Comparison Circuit)
COASEL15
OUTA
(To Fine Delay Circuit)
411

Fig. 11

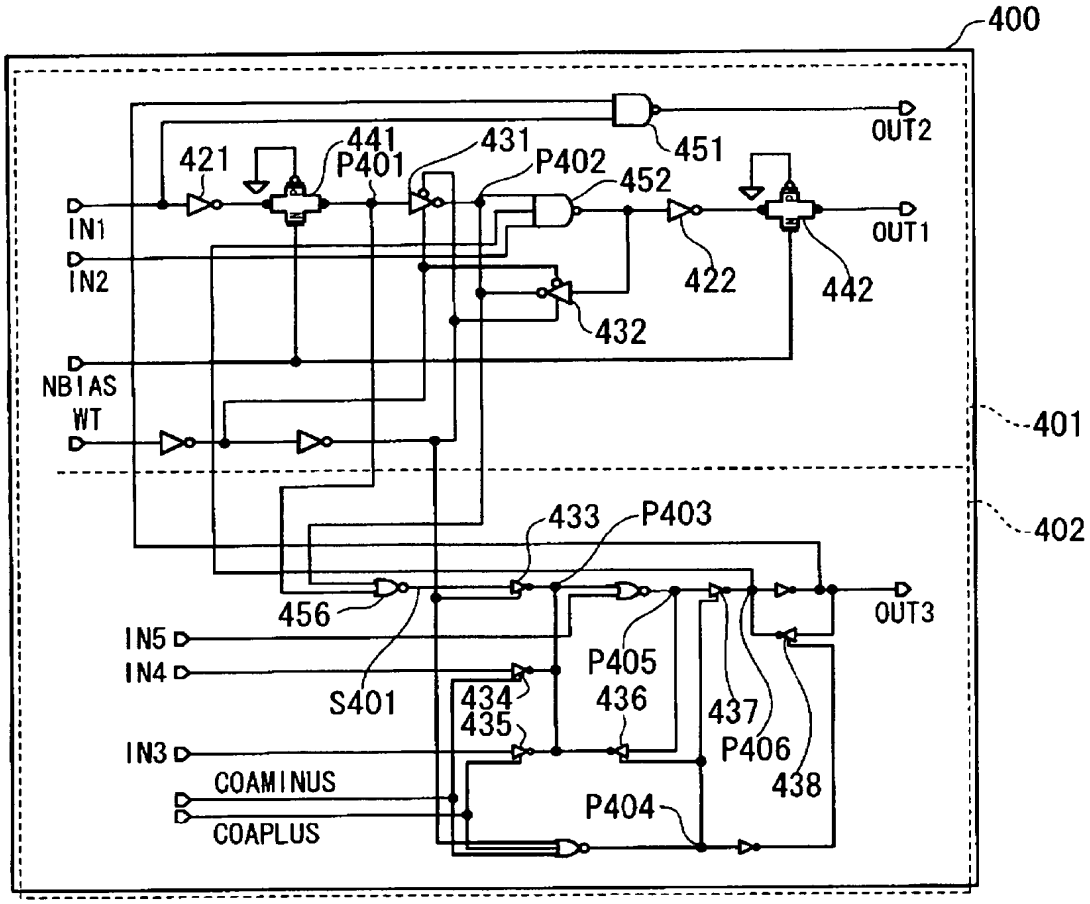
400
401
402
OUT2
OUT1
OUT3
451
452
421
441
P401
431
P402
IN1
IN2
NBIAS
WT
422
442
432
433
P403
456
IN5
IN4
IN3
COAMINUS
COAPLUS
S401
434
435
P405
436
437
P406
438
P404

Fig. 12

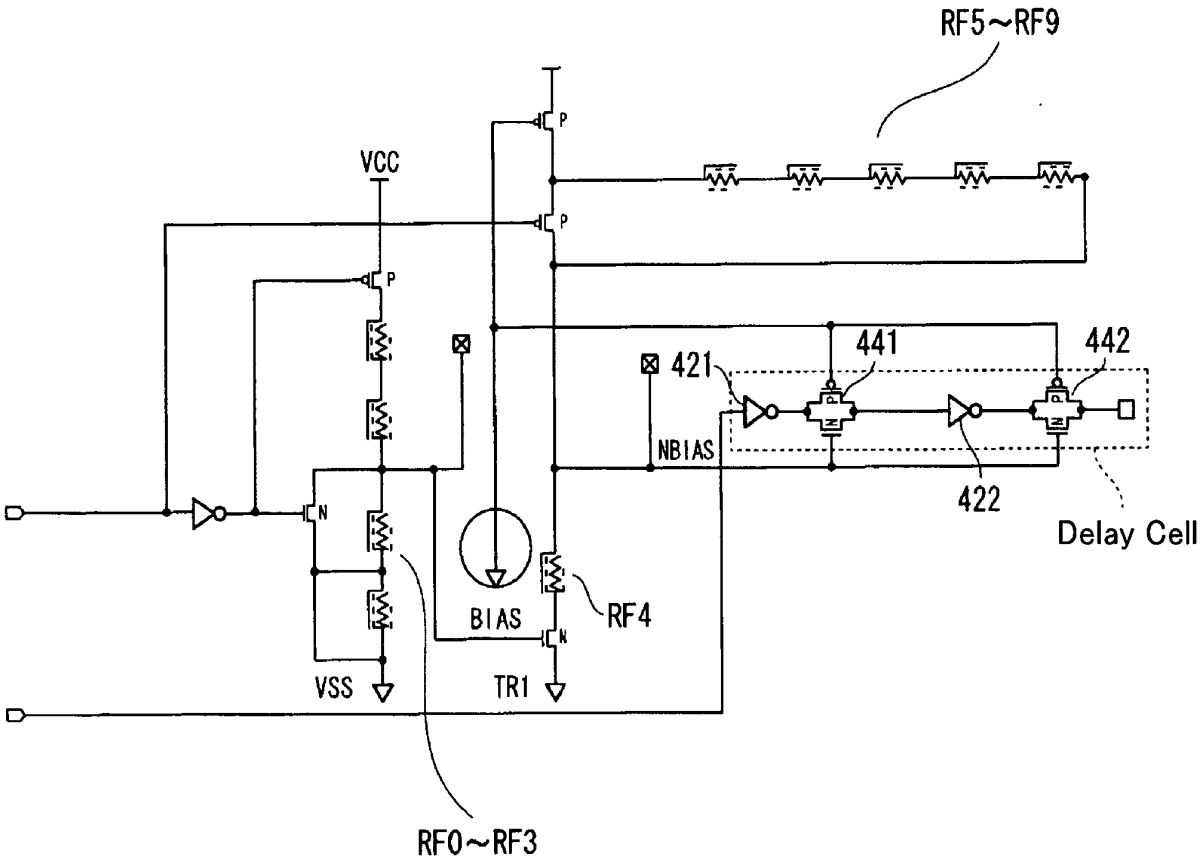
RF5~RF9
VCC
P
P
P
441
442
421
NBIAS
422
Delay Cell
N
BIAS
RF4
N
VSS
TR1
RF0~RF3

Fig. 13

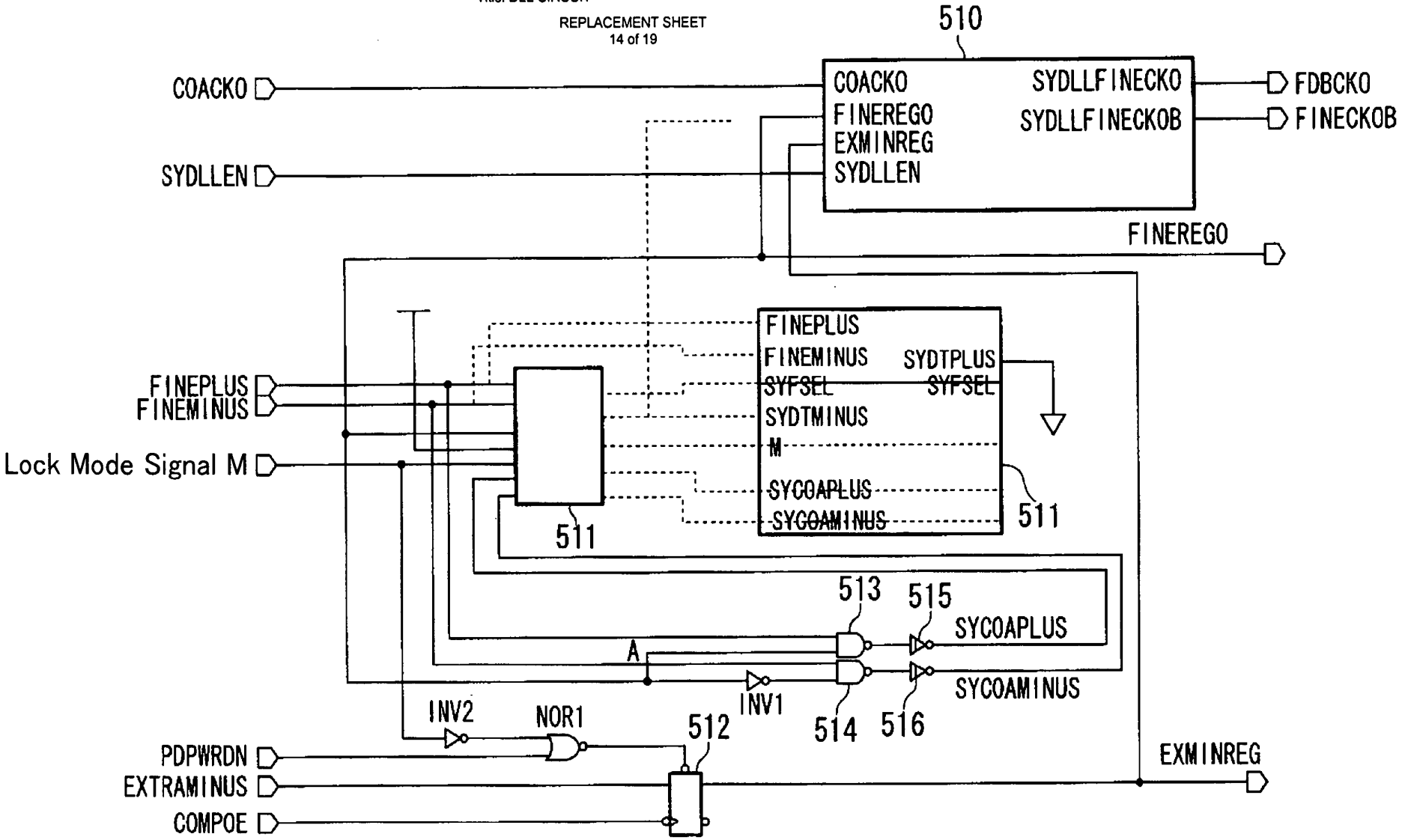
510
COACKO
SYDLLEN
COACKO
FINEREGO
EXMINREG
SYDLLEN
SYDLLFINECKO
SYDLLFINECKOB
FDBCKO
FINECKOB
FINEREGO
FINEPLUS
FINEMINUS
Lock Mode Signal M
FINEPLUS
FINEMINUS
SYFSEL
SYDTMINUS
M
SYCOAPLUS
SYCOAMINUS
SYDTPLUS
SYFSEL
511
511
513
515
SYCOAPLUS
A
SYCOAMINUS
INV1
INV2
NOR1
512
514
516
PDPWRDN
EXTRAMINUS
COMPOE
EXMINREG

Fig. 14

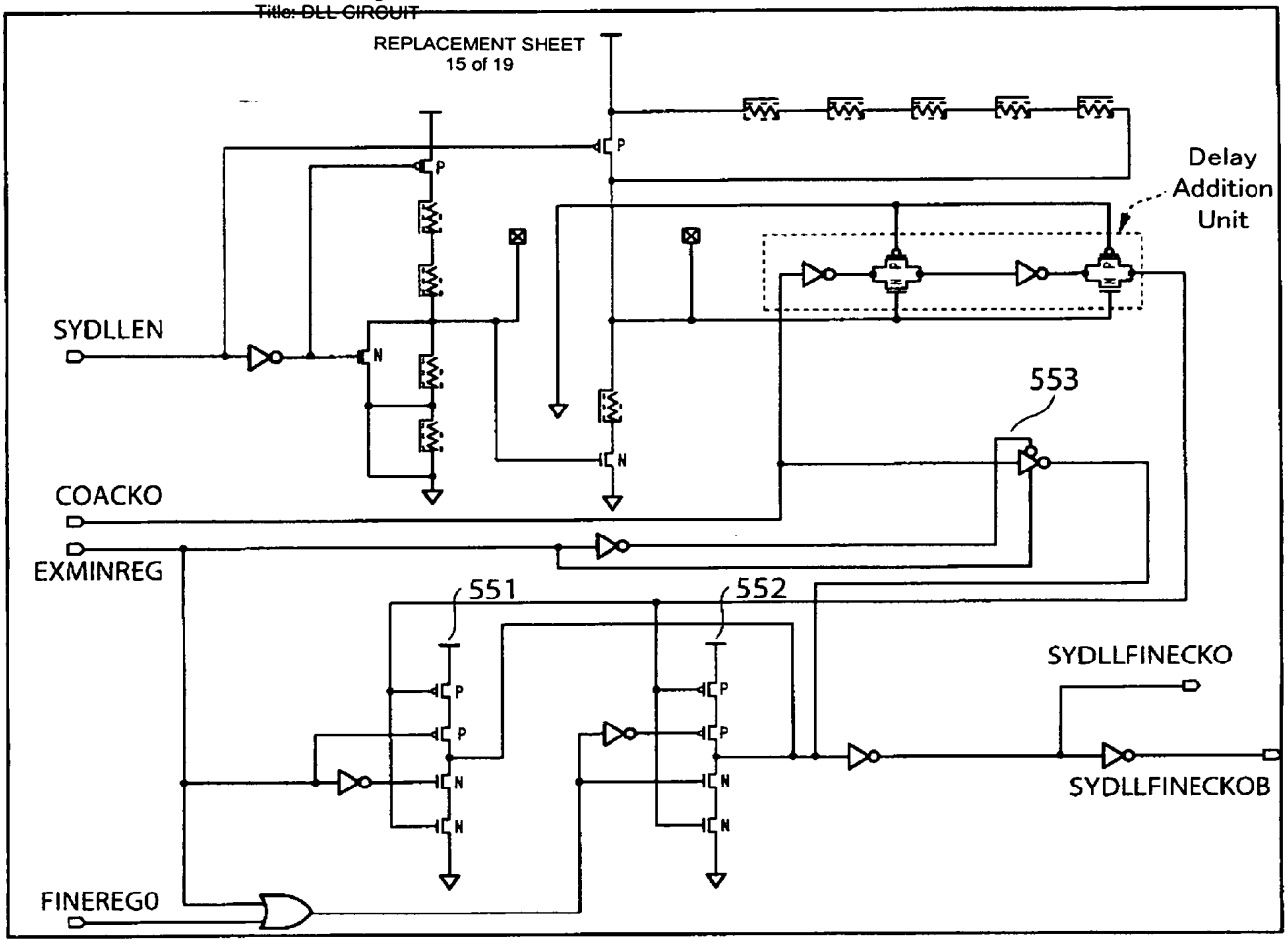
Delay
Addition
Unit
SYDLLEN
553
COACKO
EXMINREG
551
552
SYDLLFINECKO
SYDLLFINECKOB
FINEREGO
P
N

Fig. 15

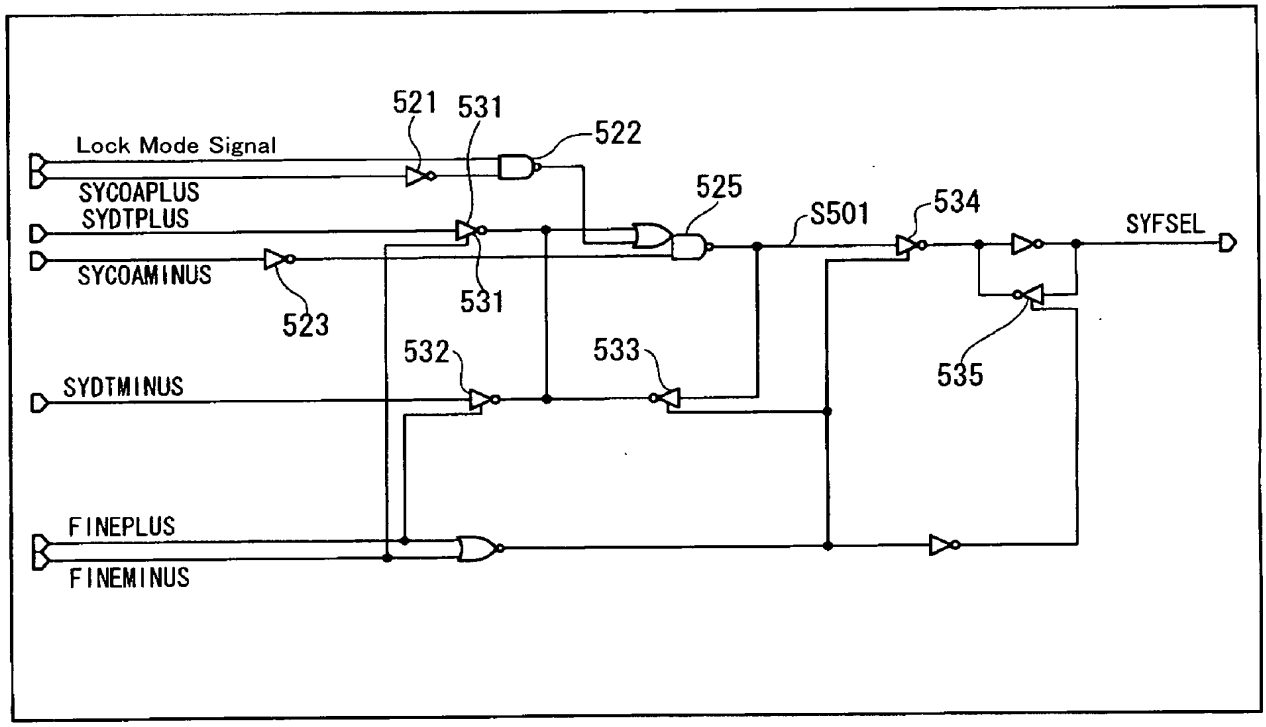
Lock Mode Signal
SYCOAPLUS
SYDTPLUS
SYCOAMINUS
SYDTMINUS
FINEPLUS
FINEMINUS
521
531
522
525
S501
534
SYFSEL
523
531
532
533
535

Fig. 16

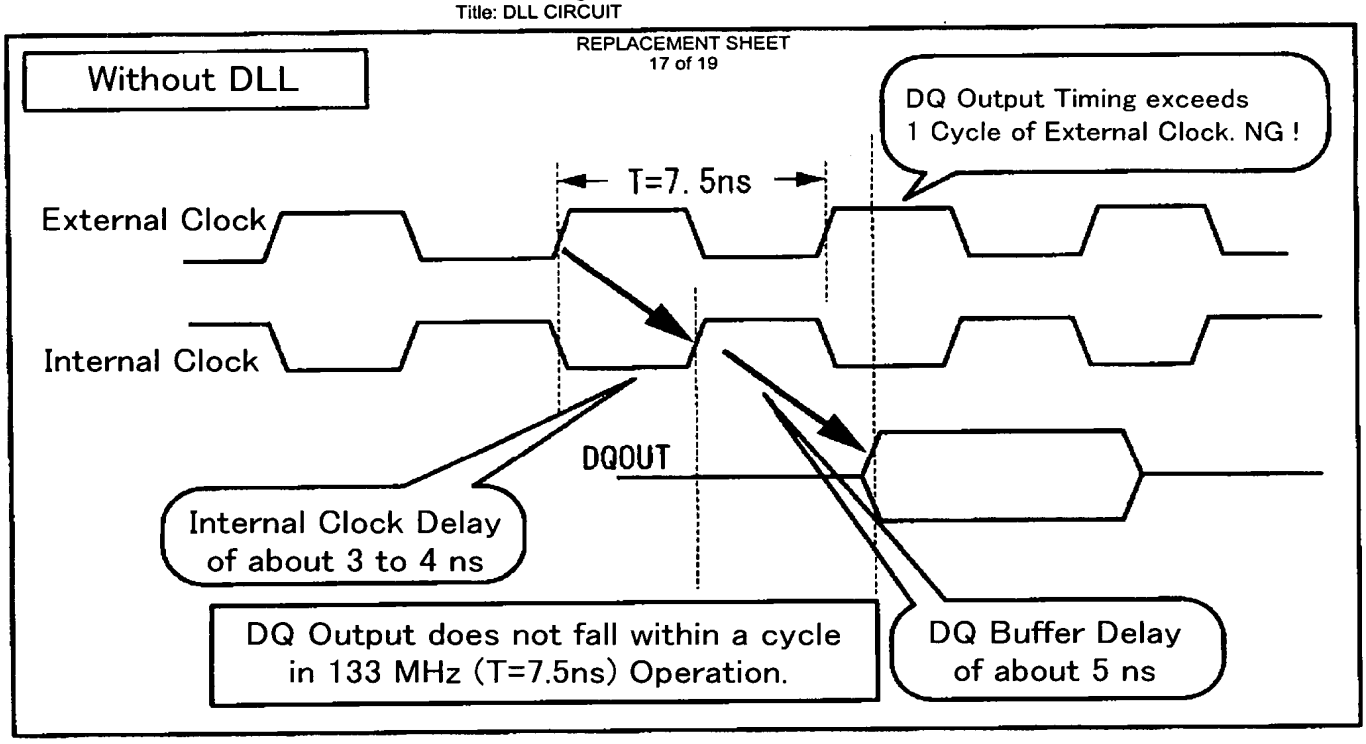

Fig. 17A

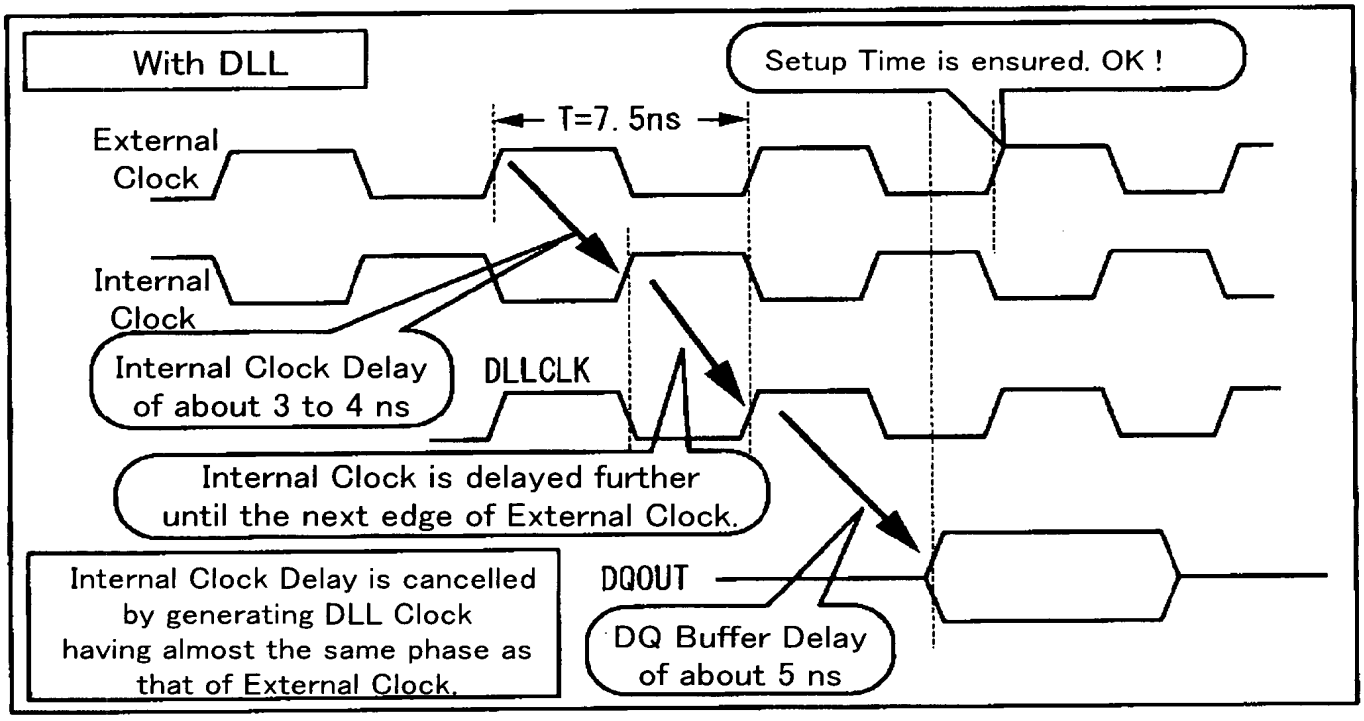

Fig. 17B

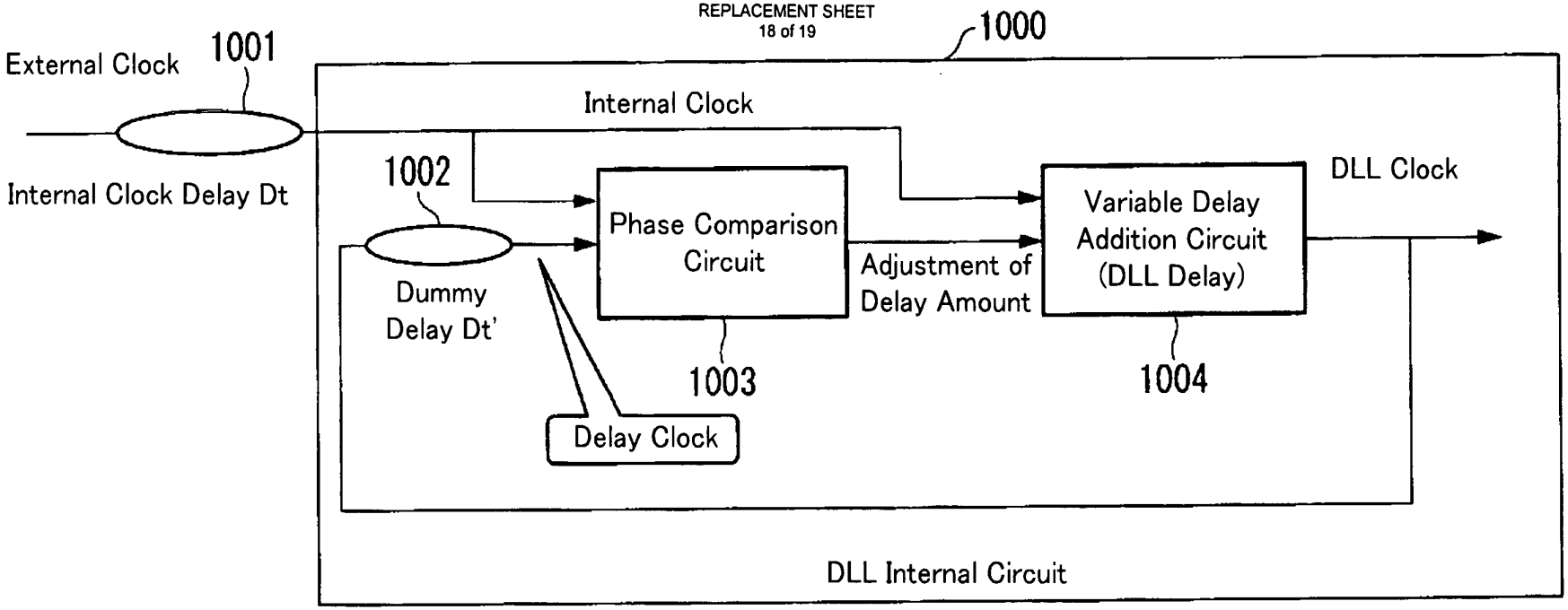
External Clock
1001
1000
Internal Clock
Internal Clock Delay Dt
1002
Phase Comparison Circuit
Variable Delay Addition Circuit (DLL Delay)
DLL Clock
Adjustment of Delay Amount
Dummy Delay Dt'
1003
1004
Delay Clock
DLL Internal Circuit

Fig. 18

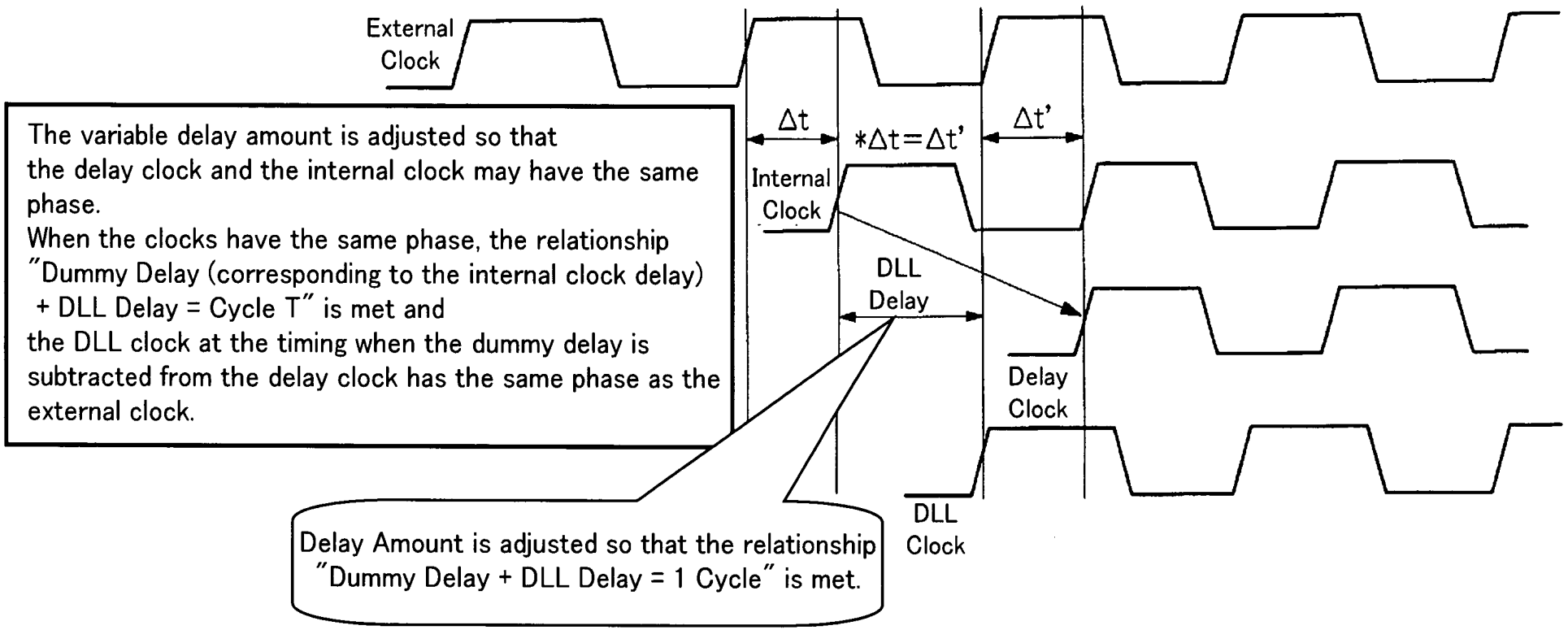
External Clock
Δt
*Δt=Δt'
Δt'
Internal Clock
DLL Delay
Delay Clock
DLL Clock
The variable delay amount is adjusted so that the delay clock and the internal clock may have the same phase.
When the clocks have the same phase, the relationship "Dummy Delay (corresponding to the internal clock delay) + DLL Delay = Cycle T" is met and the DLL clock at the timing when the dummy delay is subtracted from the delay clock has the same phase as the external clock.
Delay Amount is adjusted so that the relationship "Dummy Delay + DLL Delay = 1 Cycle" is met.

Fig. 19